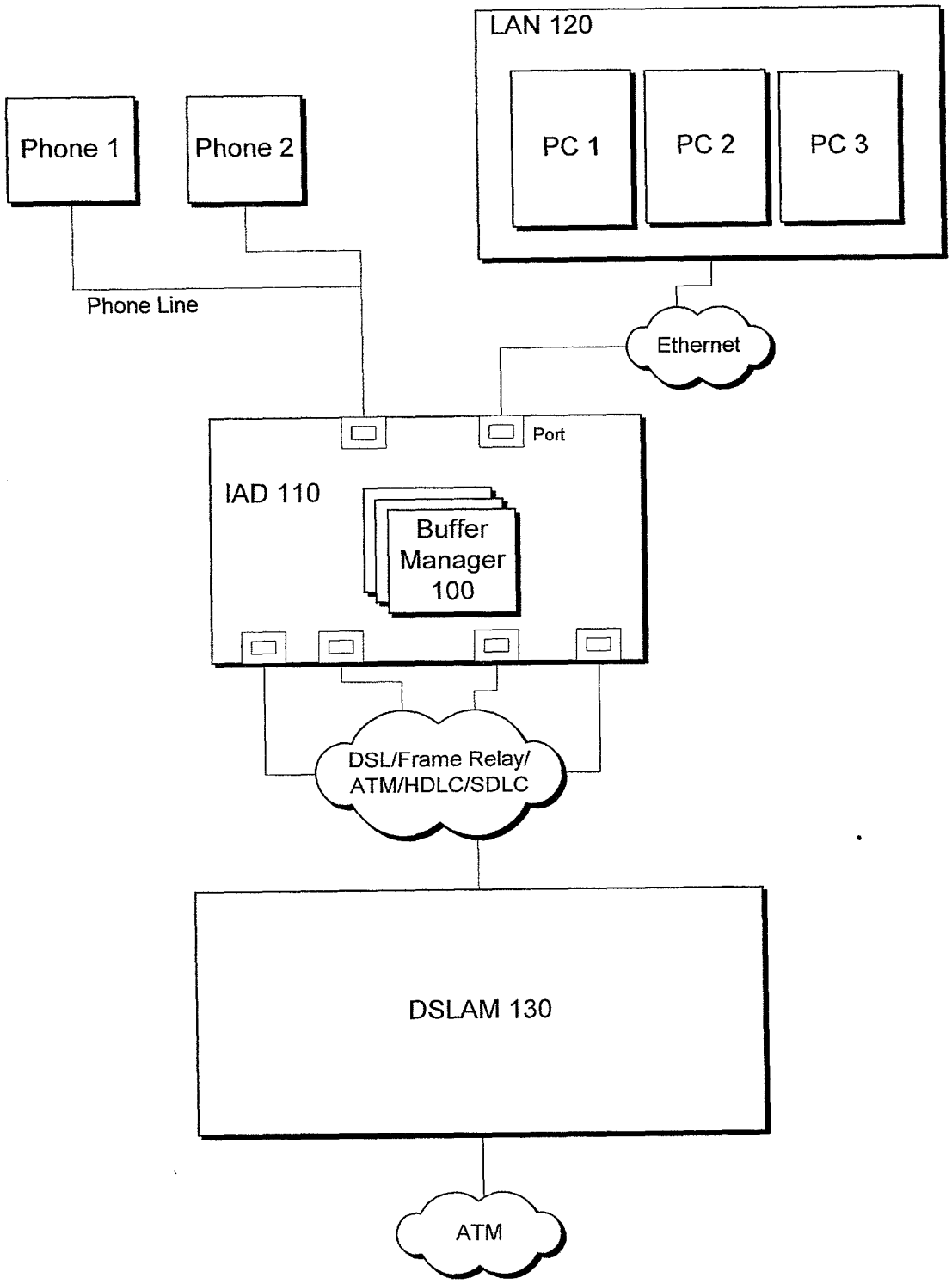

LAN 120
PC 1
PC 2
PC 3
Phone 1
Phone 2
Phone Line
Ethernet
Port
IAD 110
Buffer Manager 100
DSL/Frame Relay/ ATM/HDLC/SDLC
DSLAM 130
ATM

FIG. 1

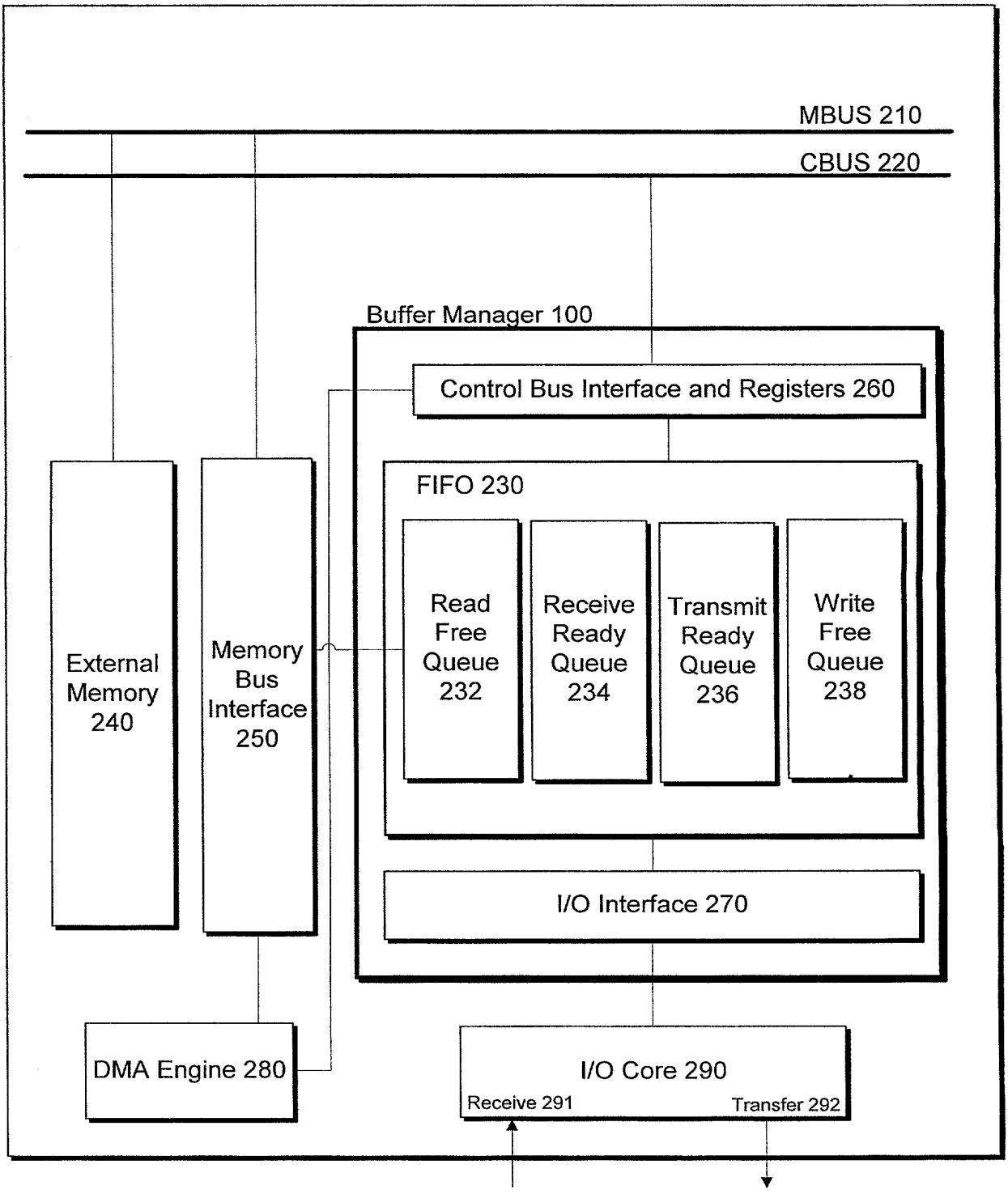

MBUS 210
CBUS 220
Buffer Manager 100
Control Bus Interface and Registers 260
FIFO 230
Read Free Queue 232
Receive Ready Queue 234
Transmit Ready Queue 236
Write Free Queue 238
External Memory 240
Memory Bus Interface 250
I/O Interface 270
DMA Engine 280
I/O Core 290
Receive 291
Transfer 292

FIG. 2

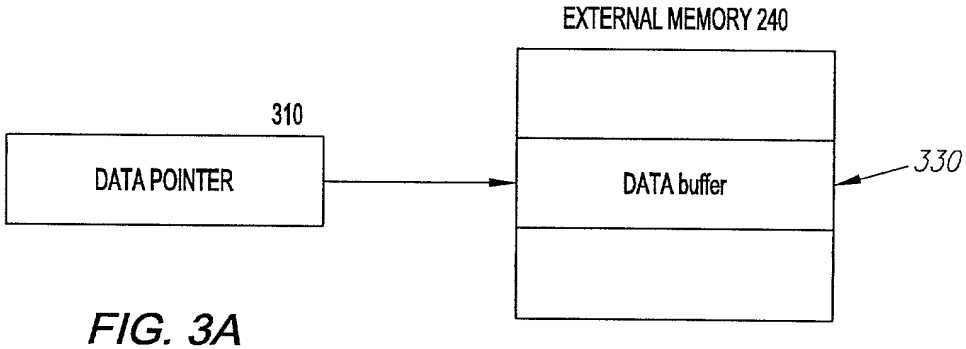


FIG. 3A

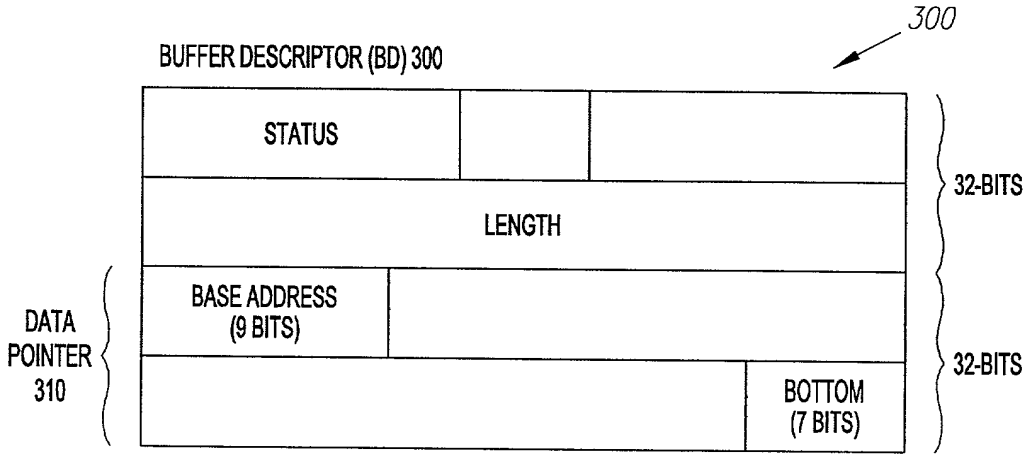
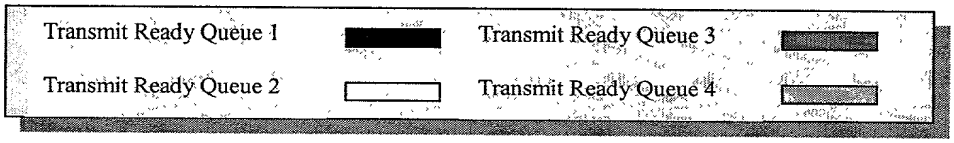


FIG. 3B

Configuration	Bit 8	Bit 7	Transmit Queue #	Depth
1	0	0	1-4	32
2	0	1	1-2	40
			3-4	24
3	1	0	1	80
			2-3	24
			4	0
4	1	1	1	64
			2	64
			3	0
			4	0

Transmit Ready Queue Configuration



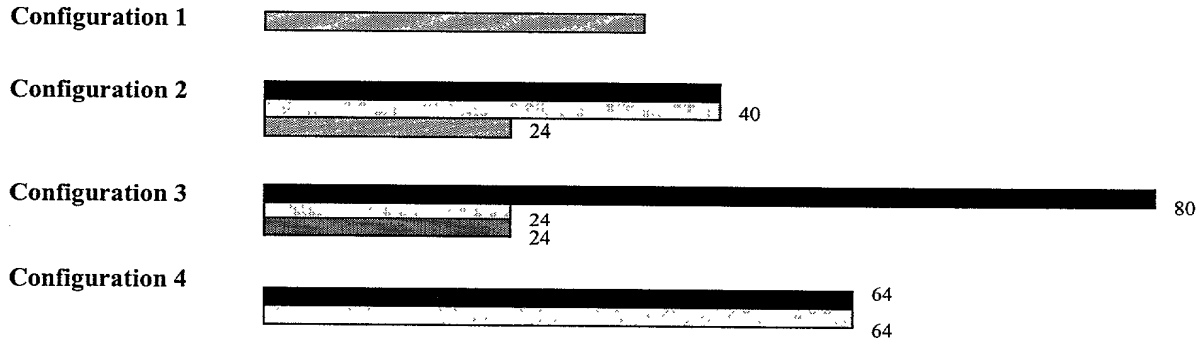


FIG. 4

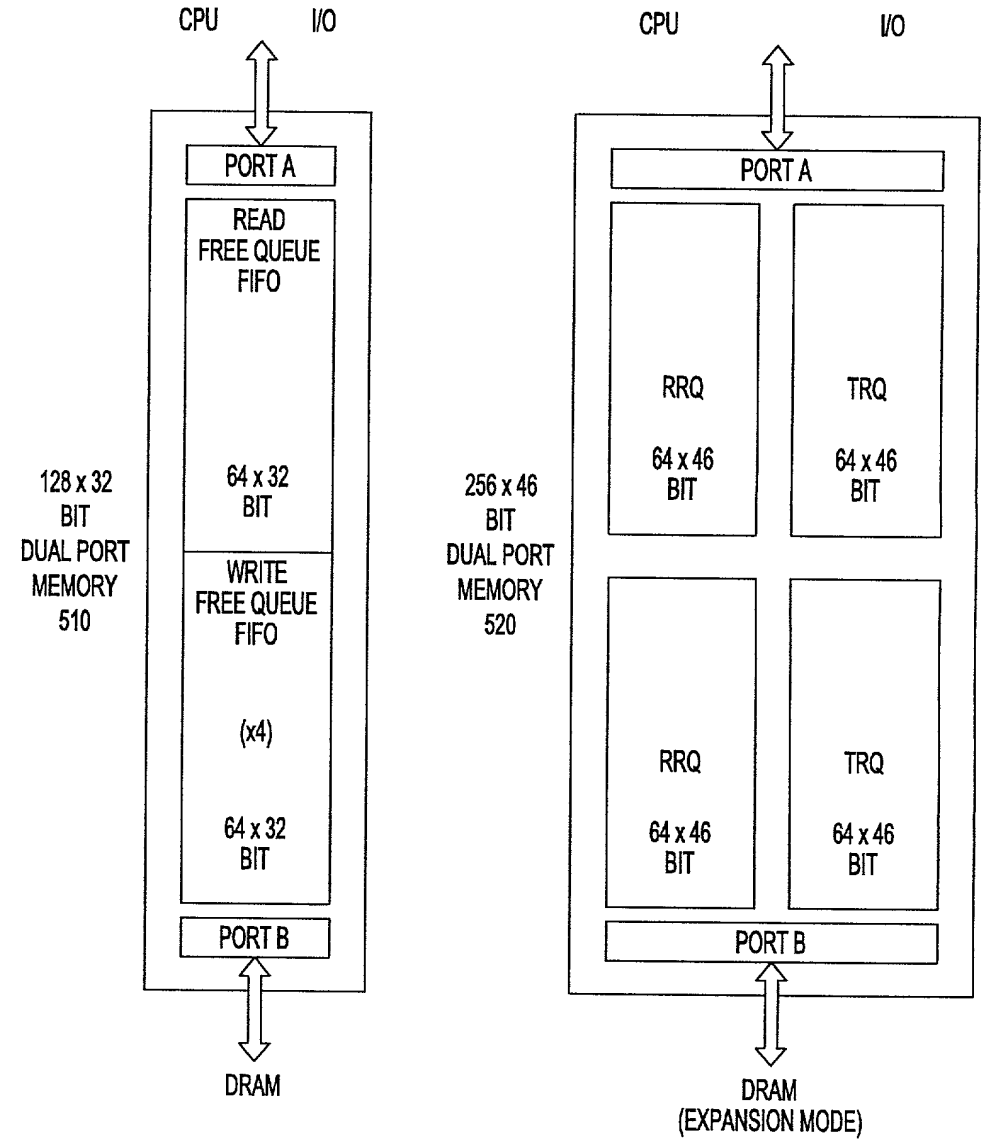


FIG. 5

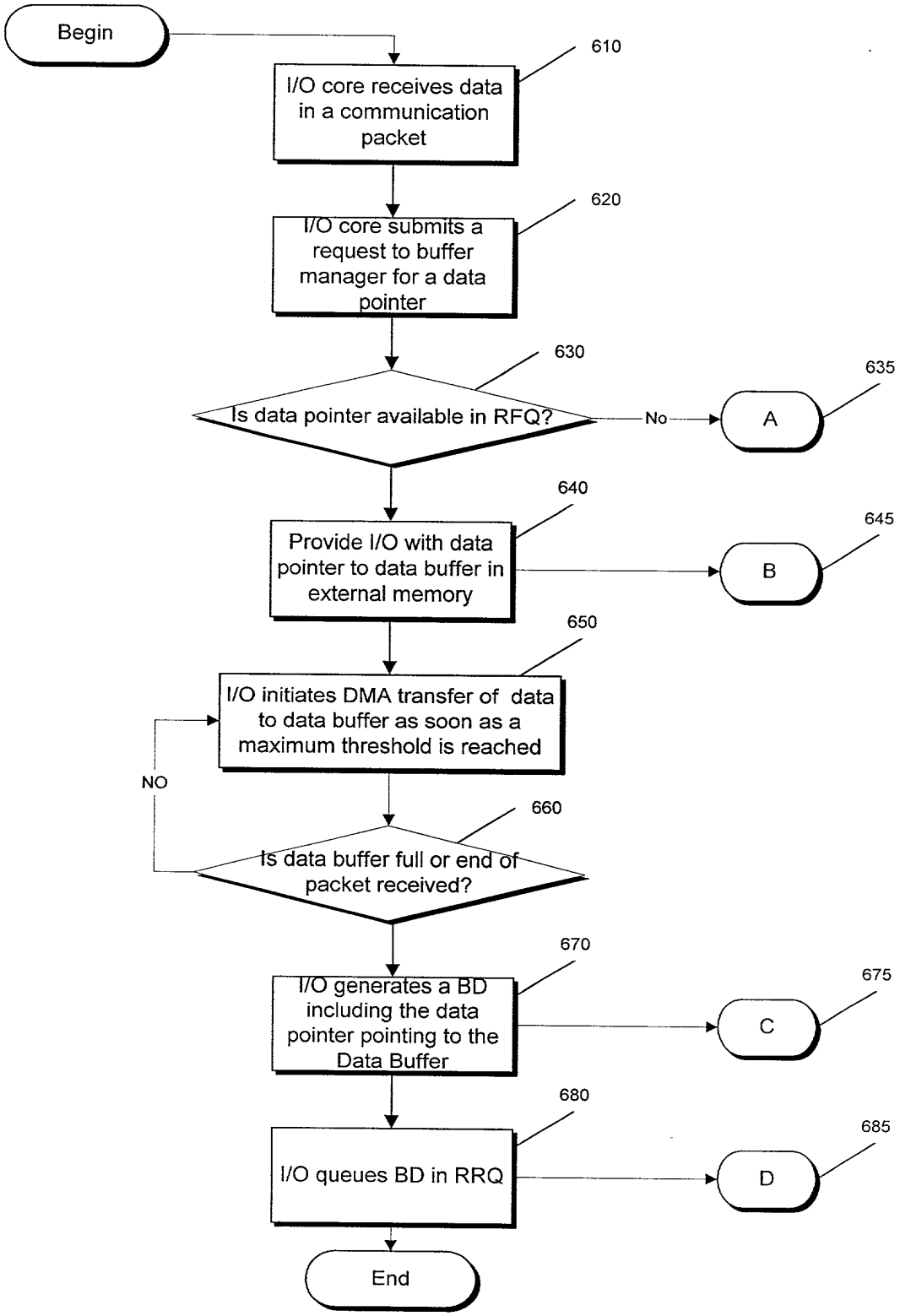

Begin
610
I/O core receives data in a communication packet
620
I/O core submits a request to buffer manager for a data pointer
630
Is data pointer available in RFQ?
No
635
A
640
Provide I/O with data pointer to data buffer in external memory
645
B
650
I/O initiates DMA transfer of data to data buffer as soon as a maximum threshold is reached
NO
660
Is data buffer full or end of packet received?
670
I/O generates a BD including the data pointer pointing to the Data Buffer
675
C
680
I/O queues BD in RRQ
685
D
End

FIG.6

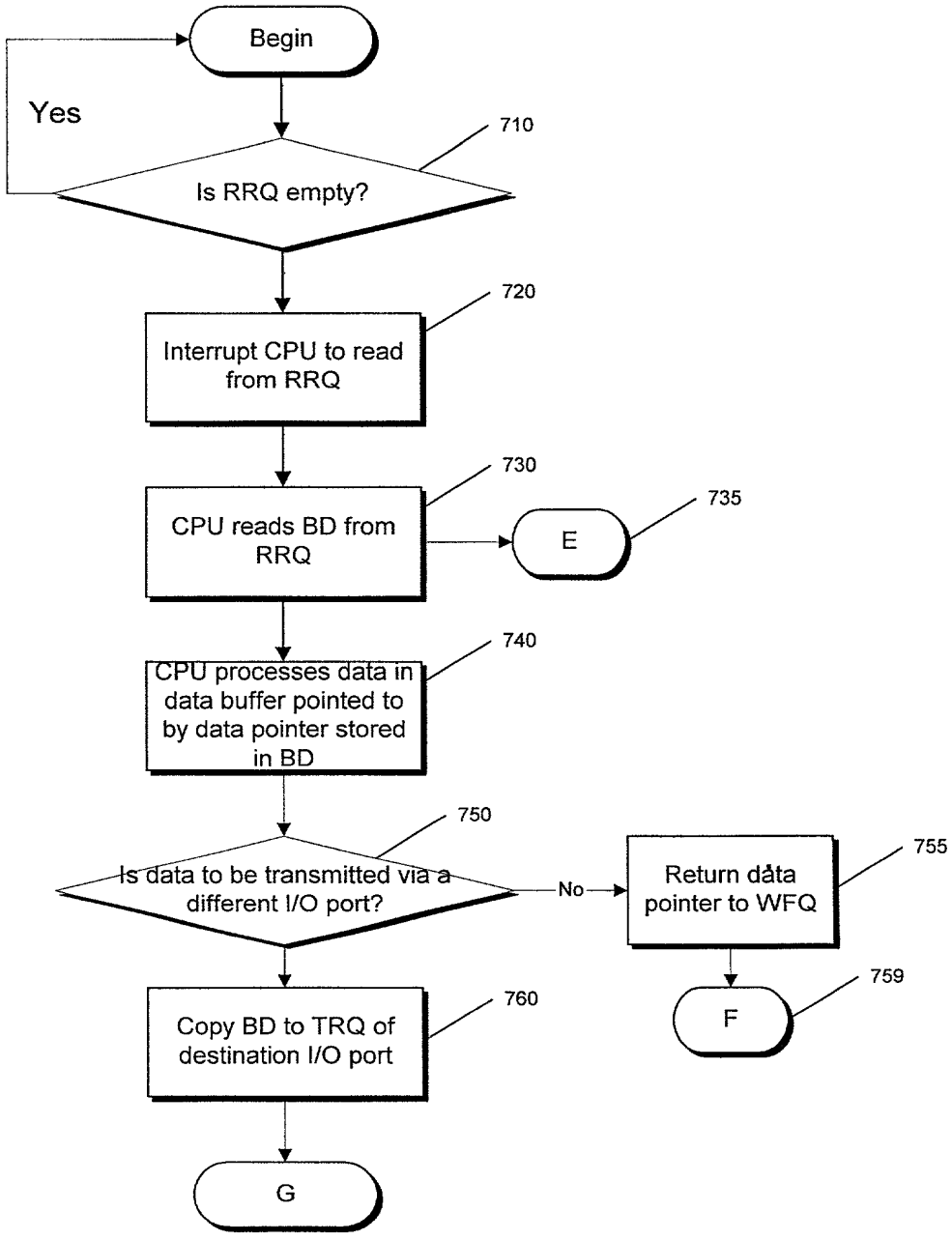


FIG. 7

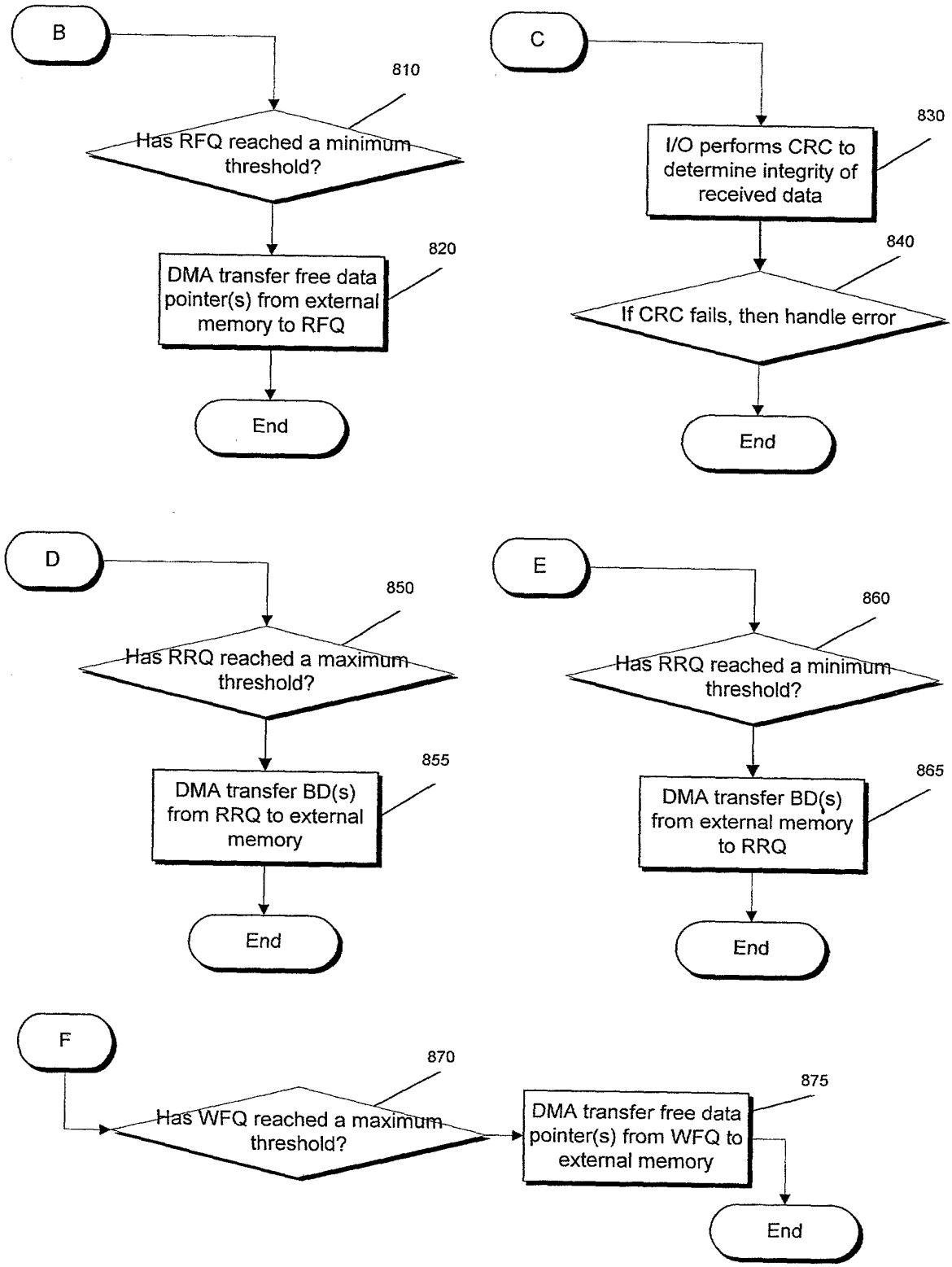


FIG.8

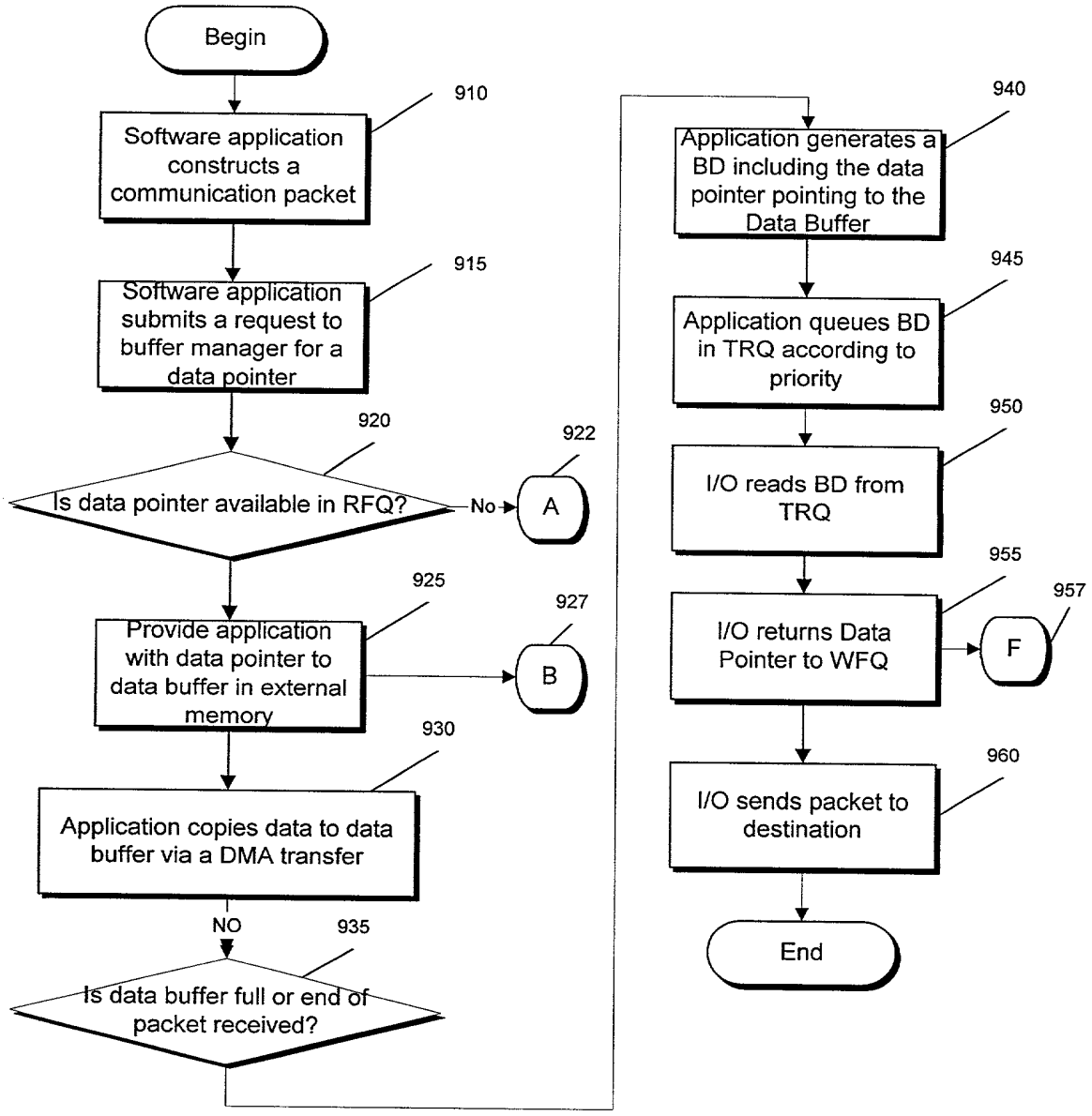

Begin
910
Software application constructs a communication packet
915
Software application submits a request to buffer manager for a data pointer
920
Is data pointer available in RFQ?
No
922
A
925
Provide application with data pointer to data buffer in external memory
927
B
930
Application copies data to data buffer via a DMA transfer
NO
935
Is data buffer full or end of packet received?
940
Application generates a BD including the data pointer pointing to the Data Buffer
945
Application queues BD in TRQ according to priority
950
I/O reads BD from TRQ
955
I/O returns Data Pointer to WFQ
957
F
960
I/O sends packet to destination
End

FIG.9

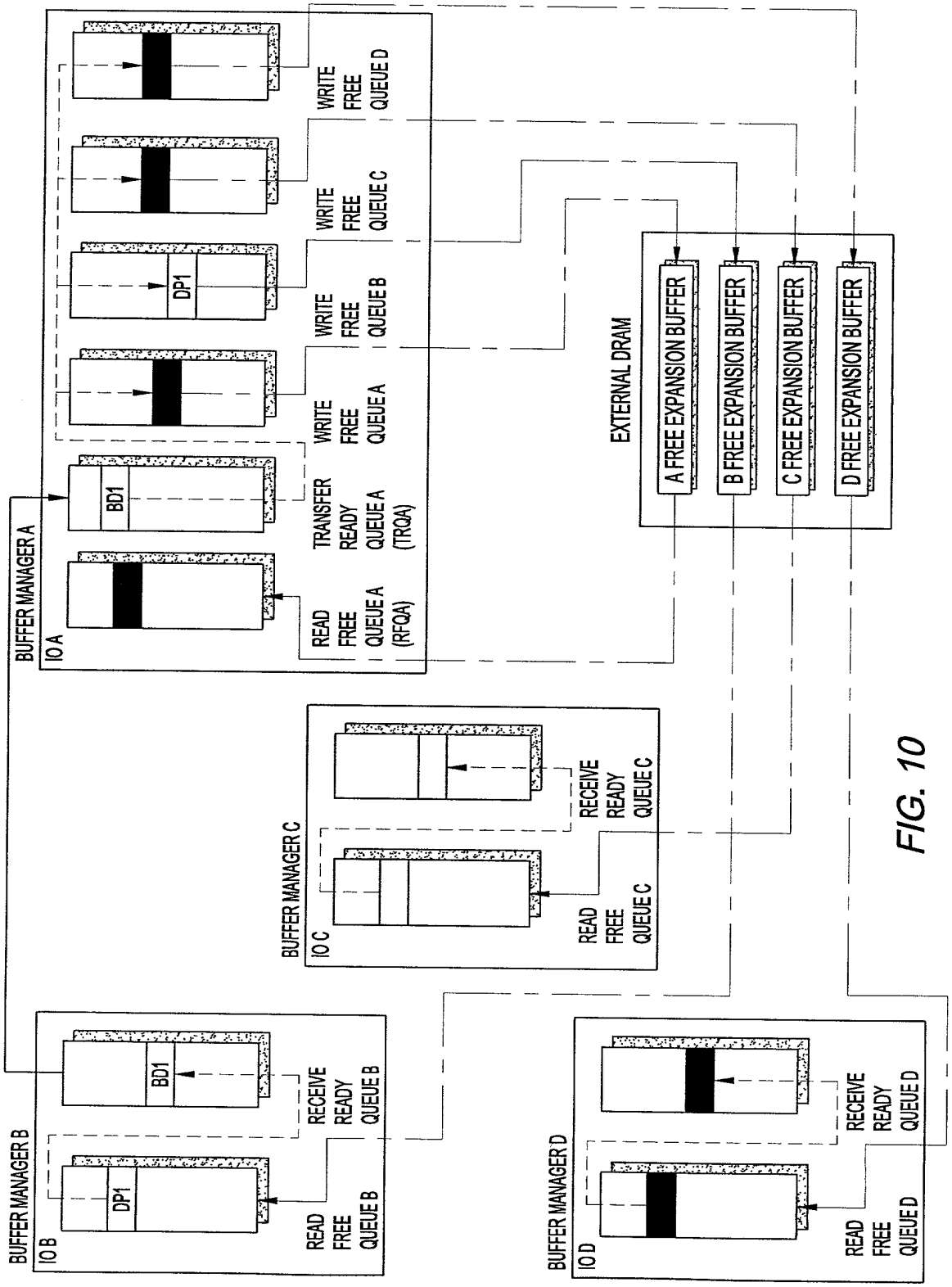


FIG. 10

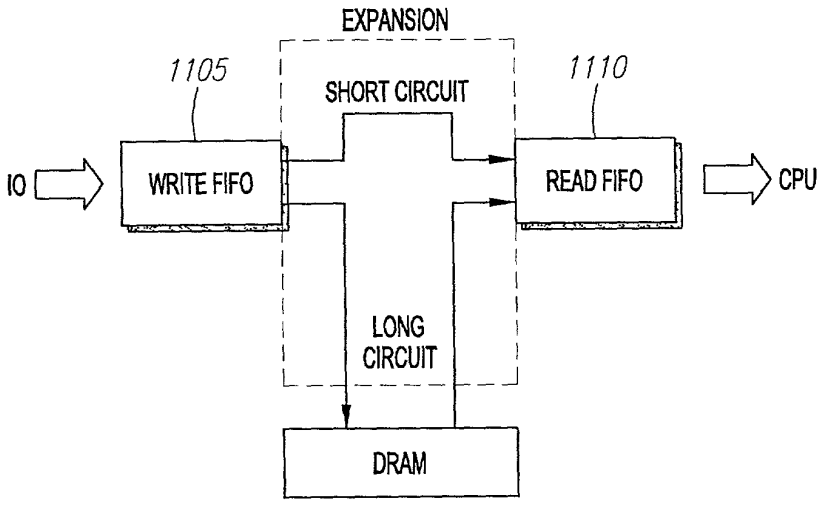

EXPANSION
1105
SHORT CIRCUIT
1110
IO
WRITE FIFO
READ FIFO
CPU
LONG CIRCUIT
DRAM

FIG. 11

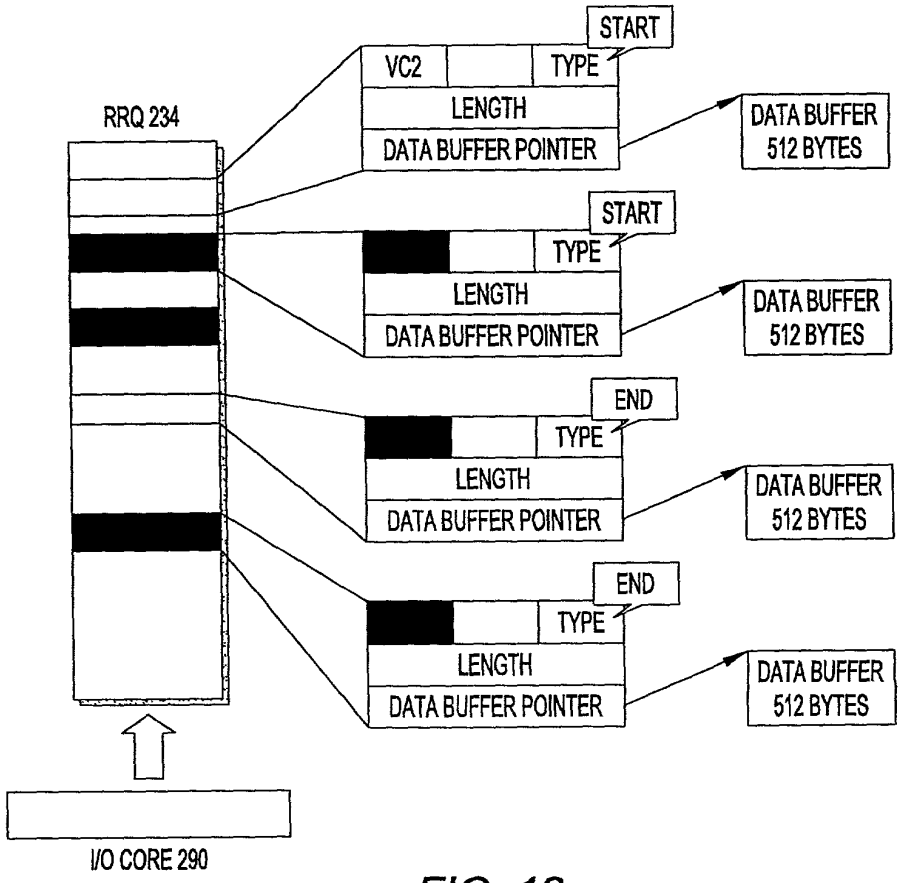

RRQ 234
START
VC2
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
START
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
END
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
END
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
I/O CORE 290

FIG. 12

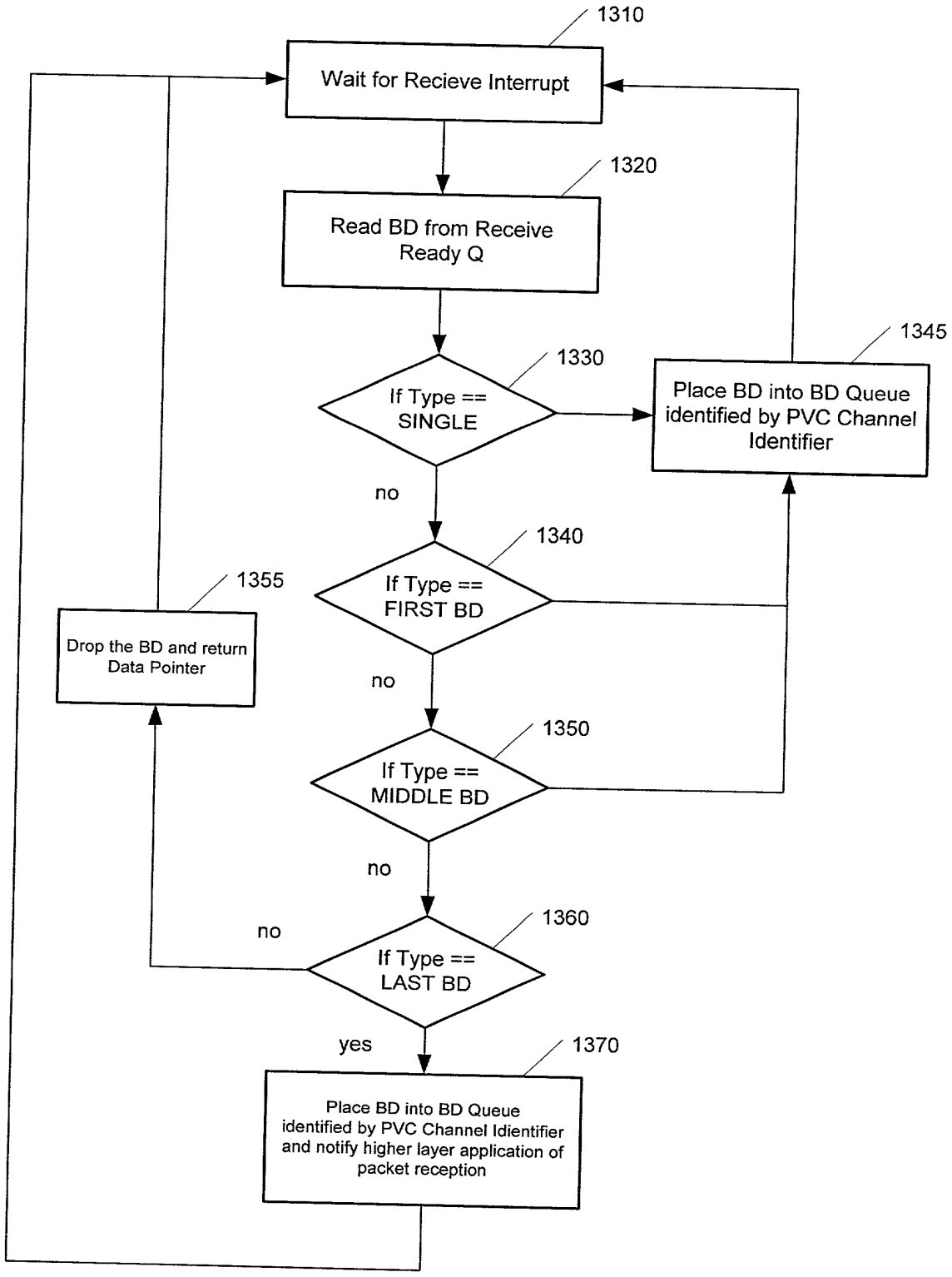

1310
Wait for Recieve Interrupt
1320
Read BD from Receive Ready Q
1330
If Type == SINGLE
1345
Place BD into BD Queue identified by PVC Channel Identifier
no
1340
If Type == FIRST BD
1355
Drop the BD and return Data Pointer
no
1350
If Type == MIDDLE BD
no
1360
If Type == LAST BD
no
yes
1370
Place BD into BD Queue identified by PVC Channel Idientifier and notify higher layer application of packet reception

FIG. 13

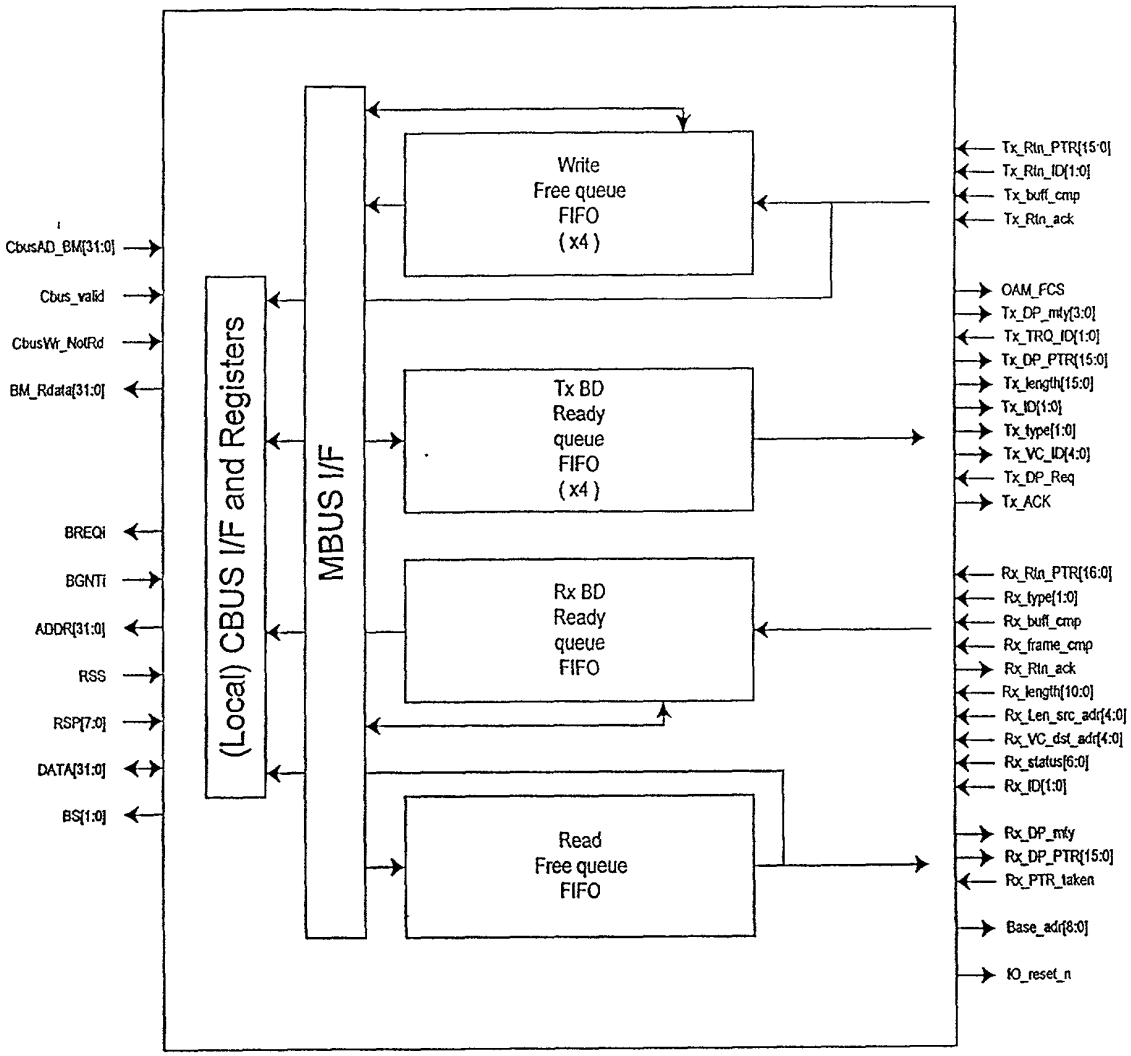

CbusAD_BM[31:0]
Cbus_valid
CbusWr_NotRd
BM_Rdata[31:0]
BREQi
BGNTi
ADDR[31:0]
RSS
RSP[7:0]
DATA[31:0]
BS[1:0]
(Local) CBUS I/F and Registers
MBUS I/F
Write Free queue FIFO (x4)
Tx BD Ready queue FIFO (x4)
Rx BD Ready queue FIFO
Read Free queue FIFO
Tx_Rtn_PTR[15:0]
Tx_Rtn_ID[1:0]
Tx_buff_cmp
Tx_Rtn_ack
OAM_FCS
Tx_DP_mty[3:0]
Tx_TRQ_ID[1:0]
Tx_DP_PTR[15:0]
Tx_length[15:0]
Tx_ID[1:0]
Tx_type[1:0]
Tx_VC_ID[4:0]
Tx_DP_Req
Tx_ACK
Rx_Rtn_PTR[16:0]
Rx_type[1:0]
Rx_buff_cmp
Rx_frame_cmp
Rx_Rtn_ack
Rx_length[10:0]
Rx_Len_src_adr[4:0]
Rx_VC_dst_adr[4:0]
Rx_status[6:0]
Rx_ID[1:0]
Rx_DP_mty
Rx_DP_PTR[15:0]
Rx_PTR_taken
Base_adr[8:0]
IO_reset_n

FIG. 14